WHAT IS CLAIMED IS:

1. A method for synthesizing a circuit representation into a new circuit representation having greater unateness, the method comprising:

(i) partitioning the circuit representation to obtain a representation of at least one sub-circuit;

(ii) recursively decomposing the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit; and

(iii) merging the sum-of-products or product-of-sums representation into the circuit representation to form a new circuit representation.

2. The method of claim 1 additionally comprising repeating steps (i), (ii) and (iii) until a desired level of unateness for the new circuit representation has been achieved.

3. The method of claim 1 wherein the sum-of-products or product-of-sums representation selected for each decomposition is the representation having fewer binate variables.

4. The method of claim 1 additionally comprising merging common expressions of the sum-of-products or product-of-sums representations.

5. The method of claim 4 wherein algebraic division is implemented to merge common unate expressions of the sum-of-products or product-of-sums representation.

6. The method of claim 1 wherein the circuit is a digital circuit.

7. The method of claim 1 wherein the representation of the at least one sub-circuit is highly unate.

8. The method of claim 1 wherein a binary decision diagram is employed to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

9. The method of claim 8 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

10. A system for synthesizing a circuit representation into a new circuit representation having greater unateness, the system comprising a computing device configured to:

(i) receive input defining the circuit representation;

(ii) partition the circuit representation to obtain a representation of at least one sub-circuit;

(iii) recursively decompose the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit;

(iv) merge the sum-of-products or product-of-sums representation into the circuit representation to form the new circuit representation; and

(v) output the new circuit representation.

11. The system of claim 10 wherein the computing device is additionally configured to:

receive input defining a desired level of unateness for the new circuit representation; and

repeat steps (ii), (iii) and (iv) until the desired level of unateness is achieved.

12. The system of claim 10 wherein the computing device is additionally configured to, for each decomposition, select the sum-of-products or product-of-sums representation having fewer binate variables.

13. The system of claim 10 wherein the computing device is additionally configured to merge common expressions of the sum-of-products or product-of-sums representations.

14. The system of claim 13 wherein the computing device is additionally configured to implement algebraic division to merge common expressions.

15. The system of claim 10 wherein the circuit is a digital circuit.

16. The system of claim 10 wherein the representation of the at least one sub-circuit is highly unate.

17. The system of claim 10 wherein the computing device is additionally configured to employ a binary decision diagram to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

18. The system of claim 17 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

19. The system of claim 10 wherein the circuit representation and the new circuit representation are input and output in a hardware description language.

20. A system for synthesizing a circuit representation into a new circuit representation having greater unateness, the system comprising:

(i) a means for receiving input defining the circuit representation;

(ii) a means for partitioning the circuit representation to obtain a representation of at least one sub-circuit;

(iii) a means for recursively decomposing the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit;

(iv) a means for merging the sum-of-products or product-of-sums representation into the circuit representation to form the new circuit representation; and

(v) a means for outputting the new circuit representation.

21. The system of claim 20 additionally comprising:

a means for receiving input defining a desired level of unateness for the new circuit representation; and

a means for repeating steps (ii), (iii) and (iv) until the desired level of unateness is achieved.

22. The system of claim 20 additionally comprising a means for selecting, for each decomposition, the sum-of-products or product-of-sums representation having fewer binate variables.

23. The system of claim 20 additionally comprising a means for merging common expressions of the sum-of-products or product-of-sums representations.

24. The system of claim 20 additionally comprising a means for implementing algebraic division to merge common expressions.

25. The system of claim 20 additionally comprising a means for partitioning the circuit representation such that the representation of the at least one sub-circuit is highly unate.

26. The system of claim 20 additionally comprising a means for employing a binary decision diagram to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

27. The system of claim 26 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

28. The system of claim 20 wherein the circuit representation and the new circuit representation are input and output in a hardware description language.

29. A computer-readable storage medium containing computer executable code for instructing one or more computers to:

(i) receive input defining a circuit representation;

(ii) partition the circuit representation to obtain a representation of at least one sub-circuit;

(iii) recursively decompose the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit;

(iv) merge the sum-of-products or product-of-sums representation into the circuit representation to form a new circuit representation; and

(v) output the new circuit representation.

30. The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to:

receive input defining a desired level of unateness for the new circuit representation; and

repeat steps (ii), (iii) and (iv) until the desired level of unateness is achieved.

31. The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to, for each decomposition, select the sum-of-products or product-of-sums representation having fewer binate variables.

32. The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to merge common expressions of the sum-of-products or product-of-sums representations.

33. The computer-readable storage medium of claim 32 wherein the computer executable code additionally instructs the computer(s) to implement algebraic division to merge common expressions.

34. The computer-readable storage medium of claim 29 wherein the circuit is a digital circuit.

35. The computer-readable storage medium of claim 29 wherein the representation of the at least one sub-circuit is highly unate.

36. The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to employ a binary decision diagram to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

37. The computer-readable storage medium of claim 36 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

38. The computer-readable storage medium of claim 29 wherein the circuit representation and the new circuit representation are input and output in a hardware description language.